

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Toshifumi IWASAKI

SERIAL NO: NEW APPLICATION

GAU:

FILED: HEREWITH

EXAMINER:

FOR: METHOD OF DESIGNING SEMICONDUCTOR DEVICE ALLOWING CONTROL OF CURRENT DRIVING CAPABILITY DEPENDING ON SHAPE OF ELEMENT FORMING REGION

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.

A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.

A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

Each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

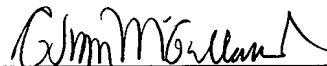
No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment form is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Marvin J. Spivak

Registration No. 24,913

C. Irvin McClelland
Registration No. 21,124



22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 05/03)

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 242006US2		SERIAL NO. NEW APPLICATION	
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Toshifumi IWASAKI			
				FILING DATE HEREWITH		GROUP	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION		
					YES	NO	
	AO	11-186495	07/09/99	Japan (with English extract)		x	
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW	Gregory SCOTT, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", IEDM, IEEE, 1999, pgs. 827-830					
	AX						
	AY						
	AZ					<input type="checkbox"/> Additional References sheet(s) attached	
Examiner				Date Considered			

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.